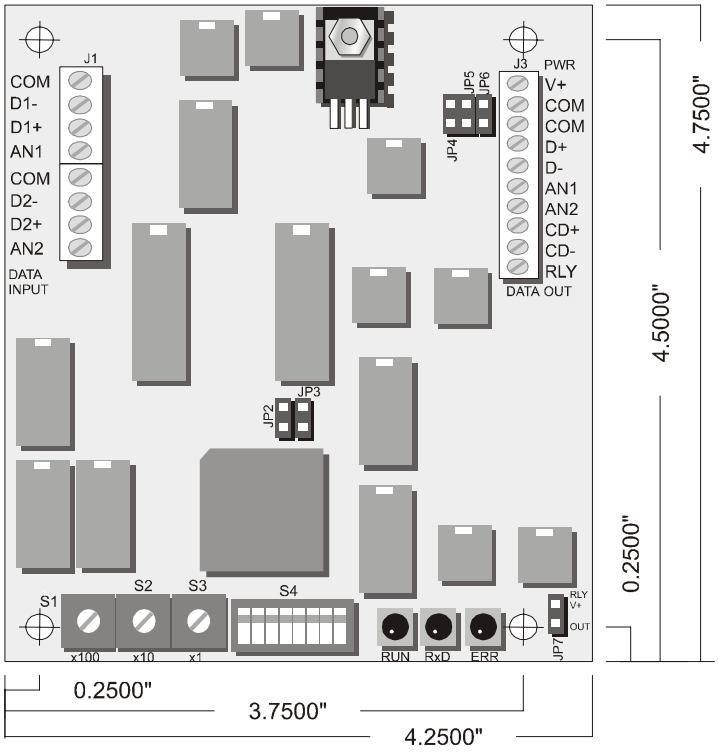
LCPM PROTOCOL MANAGER *Configuration*



CONNECTOR LEGEND

	CONNECTOR J1		CONNECTOR J3
COM	INPUT SIGNAL COMMON	**V+**	+9 to +12VDC @150mA
D1-	DMX1 DATA- / AMX1 CLOCK- INPUT	**COM**	POWER SUPPLY COMMON
D1+	DMX1 DATA+ / AMX1 CLOCK+ INPUT	**COM**	OUTPUT SIGNAL COMMON
AN1	AMX1 ANALOG INPUT	**D+**	DMX DATA+ / AMX1 CLOCK+ OUTPUT
COM	INPUT SIGNAL COMMON	**D-**	DMX DATA- / AMX1 CLOCK- OUTPUT
D2-	DMX2 DATA- / AMX2 CLOCK- INPUT	**AN1**	AMX1 ANALOG OUTPUT
D2+	DMX2 DATA+ / AMX2 CLOCK+ INPUT	**AN2**	AMX2 ANALOG OUTPUT
AN2	AMX2 ANALOG INPUT	**CD+**	AMX2 CLOCK+ OUTPUT
		CD-	AMX2 CLOCK- OUTPUT
	JUMPERS	**RLY**	RELAY DRIVE OUTPUT Open collector output used with V+ to drive external relays/ LEDs
JP1	FACTORY USE		
JP2-3	FACTORY OPTION USE		
JP4-5	Shunt for DMX OUTPUT		
	Open for AMX OUTPUT		
JP6	Open for AMX1 OUTPUT		
JP7	RELAY DRIVE OUTPUT		

LED INDICATORS

Three LEDs are used to indicate power supply and processor run status and data receive detection.

RUN Glowing steadily indicates power supply and processor OK; off indicates no power, and flashing indicates defective processor hardware.

RxD Glowing steadily indicates data 1 signal received; off indicates no signal present. Note that an address selection out of the range of the data signal will extinguish the LED.

ERR Glowing steadily indicates data 2 signal received; off indicates no signal present. Note that an address selection out of the range of the data signal will extinguish the LED.

ADDRESS SELECTION

Three rotary switches select the offset start address for the unit in most configurations. For dual AMX output, the address switches select the starting dimmer number for the second AMX output line. In test mode, the switches set dimmers to full one at a time. The switches are set as (S1) hundreds, (S2) tens

DIP SWITCH SETTINGS

OPERATING MODE	**1**	**2**
BACKUP	ON	ON
Input 1 takes priority over 2: input 2 is active on loss of 1		
PILE-ON	OFF	ON
Highest channel on each input takes precedence		
MERGE	ON	OFF
Input 2 appended to input 1 for one continuous output stream		
TEST MODES (determined by I/O mode)	OFF	OFF
Input Test: Receive data LEDs indicate correct data signal (on steadily), faulty or incorrect signal (flashing), or absence of any signal (off). **Output Test**: Desired output protocol transmitted on dimmer selected by Address Switches. Output set to full or cycled per switch 8.		

I/O MODE	**3**	**4**
DMX INPUT – DMX OUTPUT	ON	ON
DMX INPUT – AMX OUTPUT	OFF	ON
AMX INPUT – AMX OUTPUT	ON	OFF
AMX INPUT – DMX OUTPUT	OFF	OFF

DUAL AMX OUTPUT (Functional only in pile-on or backup modes)		**7**
DUAL AMX OUTPUT ENABLED		ON
DUAL AMX OUTPUT DISABLED		OFF

STATUS QUO HOLD TIME	**5**
ENABLED (5 MIN. TIME OUT)	ON
DISABLED (2 SEC. TIMEOUT)	OFF
Maintains last dimmer settings for a set time on loss of input data signal	

CALIBRATE MODE	**6**
D/A OUTPUT ENABLED Analog output level can be tested at J3-AN1 using a DC voltmeter: no other functions active	ON
D/A OUTPUT CHECK DISABLED	OFF

TEST CYCLE MODE	**8**
TEST CYCLE ENABLED Ramps the selected dimmer up and down continuously between zero and full	ON
TEST CYCLE DISABLED Sets the selected dimmer to full	OFF

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